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10/773,541	02/06/2004	Yutao Ma	188122000700	6489

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,541	MA ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 02/06/2004. Claims 1-20 are pending.

Claim Objections

1. **Claim 2** is objected to because of the following informalities: the recited "the sum of the plurality of entries is zero" needs to be clarified. Whether it refers to the entries of the current vector or the entries of the charge vector. Appropriate correction is required.

Claim 10 is objected to because of the following informalities: the recited "the system" lacks of antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5, 8, 13-14, and 16-17** are rejected under 35 U.S.C. 102(b) as being anticipated by Ahrikencheikh et al. (US Patent No. 10,773,100).

Referring to claim 1, Ahrikencheikh et al. disclose a method for evaluating a device model for a circuit element, comprising:

supplying a first set of terminal biases associated with the circuit element (col. 3, ll. 43 to col. 4, ll. 4; Fig. 4, col. 8, ll. 26 to col. 9, ll. 45, see "voltage");

obtaining a first set of model results based on the first set of terminal biases (col. 10, ll. 19 to col. 13, ll. 24); and

checking for correctness of the first set of model results by determining whether the first set of model results interrelate according to a plurality of rules (Fig. 6, col. 22, ll. 23 to col. 24, ll. 3).

Referring to claim 2, Ahrikencheikh et al. disclose the method of claim 1 wherein the first set of model results include a current vector and a charge vector having a plurality of entries, and wherein determining whether the model results interrelate according to the plurality of rules comprises determining whether the sum of the plurality of entries is zero (col. 10, ll. 19 to col. 64).

Referring to claim 3, Ahrikencheikh et al. disclose the method of claim 1 wherein the first set of model results include a charge vector having a plurality of entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the plurality of entries is zero (col. 10, ll. 19 to col. 64).

Referring to claim 4, Ahrikencheikh et al. disclose the method of claim 1 wherein the first set of model results include a conductance matrix having a plurality of rows of entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of

the entries in each of the plurality of rows of entries is zero (col. 10, ll. 19 to col. 15, ll. 35).

Referring to claim 5, Ahrikencheikh et al. disclose the method of claim 1 wherein the first set of model results include a conductance matrix having a plurality of columns of entries and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the entries in each of the plurality of columns of entries is zero (col. 10, ll. 19 to col. 15, ll. 35).

Referring to claim 8, Ahrikencheikh et al. disclose the method of claim 1 wherein the first set of model results include a conductance matrix having a plurality of diagonal entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether each diagonal entry is non-negative (col. 10, ll. 19 to col. 15, ll. 35).

Referring to claim 13, Ahrikencheikh et al. disclose a method for simulating a system having a large number of elements interconnected through their terminals, some or all of the elements are modeled by element models each for generating model results describing characteristic of an element under a set of terminal conditions; comprising:

obtaining a first set of model results associated with an element in the system based on a first set of terminal conditions for the element (Ahrikencheikh et al., col. 10, ll. 19 to col. 13, ll. 24); and

checking for correctness of the first set of model results by determining whether the first set of model results interrelate according to a plurality of rules (Ahrikencheikh et al., Fig. 6, col. 22, ll. 23 to col. 24, ll. 3).

Referring to claim 14, Ahrikencheikh et al. disclose the method of claim 13 wherein the model results are stamped into designated entries in matrices associated with a set of matrix equations that simulate the system and the method further comprising: obtaining solutions for states of the system by solving the set of matrix equations (Fig. 6, col. 10, ll. 10 to col.15, ll. 35).

Referring to claim 16, Ahrikencheikh et al. disclose a computer readable medium storing therein computer readable program instructions (Fig. 4) that, when executed by a computer, cause the computer to perform a method for evaluating a device model for a circuit element, the computer readable program instructions comprising:

instructions for supplying a first set of terminal biases (col. 3, ll. 43 to col. 4, ll. 4; Fig. 4, col. 8, ll. 26 to col. 9, ll. 45, see "voltage");

instructions for obtaining a first set of model results based on the first set of terminal biases (col. 10, ll. 19 to col. 13, ll. 24); and

instructions for checking for correctness of the first set of model results by determining whether the first set of model results interrelate according to a plurality of rules (Fig. 6, col. 22, ll. 23 to col. 24, ll. 3).

Referring to claim 17, Ahrikencheikh et al. disclose the computer readable medium of claim 16 wherein the first set of model results include a current vector and a

charge vector each having a plurality of entries, and wherein the instructions for determining whether the model results interrelate according to the plurality of rules comprises:

instructions for determining whether the sum of the plurality of entries in the current vector is zero (col. 10, ll. 19 to col. 64); and

instructions for determining whether the sum of the plurality of entries in the charge vector is zero (col. 10, ll. 19 to col. 64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 6-7, 9-10, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahrikencheikh et al. in view of Nguyen et al. (1998), "Simulation of Coupling Capacitance Using Matrix Partitioning", International Conference on Computer Aid Design (ICCD 1998), Proceedings of the 1998 IEEE/ACM International Conference on Computer-Aid Design, San Jose, California, US, pages 12-18.

Referring to claim 6, Ahrikencheikh et al. substantially disclose all the limitations of claim 6. However, **Ahrikencheikh et al. do not disclose** the first set of model results include a capacitance matrix having a plurality of rows of entries, and wherein determining whether the first set of model results interrelate according to the plurality of

rules comprises determining whether the sum of the entries in each of the plurality of rows of entries is zero.

Nguyen et al. disclose the first set of model results include a capacitance matrix having a plurality of rows of entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the entries in each of the plurality of rows of entries is zero (Nguyen et al. , section 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Nguyen et al. in order to simplify device model and speed up circuit simulation (Nguyen et al., section 3).

Referring to claim 7, Ahrikencheikh et al. substantially disclose all the limitations of claim 7. However, **Ahrikencheikh et al. do not disclose** the first set of model results include a capacitance matrix having a plurality of columns of entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the entries in each of the plurality of columns of entries is zero.

Nguyen et al. disclose the first set of model results include a capacitance matrix having a plurality of columns of entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether the sum of the entries in each of the plurality of columns of entries is zero (Nguyen et al., section 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Nguyen et al. in order to simplify device model and speed up circuit simulation (Nguyen et al., section 3).

Referring to claim 9, Ahrikencheikh et al. substantially disclose all the limitations of claim 9. However, **Ahrikencheikh et al. do not disclose** the first set of model results include a capacitance matrix having a plurality of diagonal entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether each diagonal entry is non-negative.

Nguyen et al. disclose the first set of model results include a capacitance matrix having a plurality of diagonal entries, and wherein determining whether the first set of model results interrelate according to the plurality of rules comprises determining whether each diagonal entry is non-negative (Nguyen et al., section 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Nguyen et al. in order to simplify device model and speed up circuit simulation (Nguyen et al., section 3).

Referring to claim 10, Ahrikencheikh et al. substantially disclose all the limitations of claim 10. However, **Ahrikencheikh et al. do not disclose** the first set of model results are stamped into designated positions in matrices associated with equations for simulating the system.

Nguyen et al. disclose the first set of model results are stamped into designated positions in matrices associated with equations for simulating the system (Nguyen et al., section 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Nguyen et al. in order to simplify device model and speed up circuit simulation (Nguyen et al., section 3).

Referring to claim 18, Ahrikencheikh et al. disclose all the limitations of claim 16, wherein the first set of model results include a conductance matrix and a capacitance matrix each having a plurality of rows of entries and a plurality of columns of entries, and wherein the instructions for determining whether the first set of model results interrelate according to the plurality of rules comprises:

instructions for determining whether the sum of the entries in each of the plurality of rows of entries in the conductance matrix is zero (Ahrikencheikh et al. , col. 10, ll. 19 to col. 15, ll. 35);

instructions for determining whether the sum of the entries in each of the plurality of columns of entries in the conductance matrix is zero (Ahrikencheikh et al. , col. 10, ll. 19 to col. 15, ll. 35);

However, **Ahrikencheikh et al. do not disclose**:

instructions for determining whether the sum of the entries in each of the plurality of rows of entries in the capacitance matrix is zero; instructions for determining whether the sum of the entries in each of the plurality of columns of entries in the capacitance

matrix is zero; instructions for determining whether each diagonal entry in the conductance matrix is non-negative; and instructions for determining whether each diagonal entry in the capacitance matrix is non-negative .

Nguyen et al disclose:

instructions for determining whether the sum of the entries in each of the plurality of rows of entries in the capacitance matrix is zero (Nguyen et al. , section 2);

instructions for determining whether the sum of the entries in each of the plurality of columns of entries in the capacitance matrix is zero (Nguyen et al. , section 2);

instructions for determining whether each diagonal entry in the conductance matrix is non-negative (Nguyen et al. , section 2); and

instructions for determining whether each diagonal entry in the capacitance matrix is non-negative (Nguyen et al. , section 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Nguyen et al. in order to simplify device model and speed up circuit simulation (Nguyen et al., section 3).

6. **Claims 11-12, 15, and 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahrikencheikh et al. in view of Sharrit (US Patent No. 5,588,142).

7. **Referring to claim 11,** Ahrikencheikh et al. substantially disclose the method of claim 11. However, **Ahrikencheikh et al. do not disclose** the step of checking for correctness of the first set of model results further comprises: supplying a second set of terminal biases that is slightly different from the first set of terminal biases; obtaining a

second set of model results based on the second set of terminal biases; and checking for correctness of the first set of model results based on differences between the first set of model results and the second set of model results and on differences between the first set of terminal biases and the second set of terminal biases.

Sharrit et al. disclose checking for correctness of the first set of model results further comprises:

supplying a second set of terminal biases that is slightly different from the first set of terminal biases (Sharrit, Fig. 1, col. 9, ll. 60 to col. 10, ll. 12);

obtaining a second set of model results based on the second set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30); and

checking for correctness of the first set of model results based on differences between the first set of model results and the second set of model results and on differences between the first set of terminal biases and the second set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Sharrit because the combined teachings would provide an improve method for simulating an electronic circuit on a computer (Sharrit, col. 4, ll. 9-11)

Referring to claim 12, Ahrikencheikh et al. substantially disclose the method of claim 12. However, **Ahrikencheikh et al. do not disclose** the step of all except one of the second set of terminal biases are equal to respective ones of the first set of terminal biases.

Sharrit disclose the step of all except one of the second set of terminal biases are equal to respective ones of the first set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Sharrit because the combined teachings would provide an improve method for simulating an electronic circuit on a computer (Sharrit, col. 4, ll. 9-11).

Referring to claim 15, Ahrikencheikh et al. substantially disclose the method of claim 15. However, **Ahrikencheikh et al. do not disclose**:

forming a second set of terminal conditions for the element based on the solutions for the states of the system; obtaining a second set of model results associated with the element based on the second set of terminal conditions for the element; and checking for correctness of the second set of model results by determining whether the second set of model results interrelate according to the plurality of rules.

Sharrit disclose forming a second set of terminal conditions for the element based on the solutions for the states of the system (Sharrit, Figs. 1-3, col. 9 to col. 11, ll. 30);

obtaining a second set of model results associated with the element based on the second set of terminal conditions for the element (Sharrit , Figs. 1-3, col. 9 to col. 11, ll. 30); and

checking for correctness of the second set of model results by determining

whether the second set of model results interrelate according to the plurality of rules (Sharrit , Figs. 1-3, col. 9 to col. 11, ll. 30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Sharrit because the combined teachings would provide an improve method for simulating an electronic circuit on a computer (Sharrit, col. 4, ll. 9-11).

Referring to claim 19, Ahrikencheikh et al. substantially disclose the limitations of claim 19. However, **Ahrikencheikh et al. do not disclose**:

instructions for supplying a second set of terminal biases that is slightly different from the first set of terminal biases; instructions for obtaining a second set of model results based on the second set of terminal biases; and instructions for checking for correctness of the first set of model results based on differences between the first set of model results and the second set of model results and on differences between the first set of terminal biases and the second set of terminal biases.

Sharrit disclose:

the instructions for checking for correctness of the first set of model results further comprises:

instructions for supplying a second set of terminal biases that is slightly different from the first set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30);

instructions for obtaining a second set of model results based on the second set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30); and

instructions for checking for correctness of the first set of model results based on differences between the first set of model results and the second set of model results and on differences between the first set of terminal biases and the second set of terminal biases (Sharrit , Figs. 1-3, col. 9 to col. 11, ll. 30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ahrikencheikh et al. with the teachings disclosed by Sharrit because the combined teachings would provide an improve method for simulating an electronic circuit on a computer (Sharrit, col. 4, ll. 9-11).

Referring to claim 20, the computer readable medium of claim 19 wherein all except one of the second set of terminal biases are equal to respective ones of the first set of terminal biases (Sharrit, Figs. 1-3, col. 9, ll. 60 to col. 11, ll. 30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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